Homework 4

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Due before class on March 25

1. [20pts]Consider the following loop.

Loop: lw r1, 0(r1)

and r1, r1, r2

lw r1, 0(r1)

lw r1, 0(r1)

beq r1, r0, loop

Assume that perfect branch prediction is used (no stalls due to control hazards), that there are no delay slots, and that the pipeline has full forwarding support. Also assume that many iterations of this loop are executed before the loop exits.

1. [15pts]Show a pipeline execution diagram for the third iteration of this loop, from the cycle in which we fetch the first instruction of that iteration up to (but not including) the cycle in which we can fetch the first instruction of the next iteration. Show all instructions that are in the pipeline during these cycles (not just those from the third iteration. Some from 2nd and 4th iterations).

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| (2nd) | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (2nd) | E | M | W |  |  |  |  |  |  |  |  |  |  |  |  |
| (2nd) | D | E | M | W |  |  |  |  |  |  |  |  |  |  |  |
| Loop: lw r1,0(r1) | F | D | E | M | W |  |  |  |  |  |  |  |  |  |  |
| and r1, r1, r2 |  | F | D | E | M | W |  |  |  |  |  |  |  |  |  |
| lw r1, 0(r1) |  |  | F | D | E | M | W |  |  |  |  |  |  |  |  |
| lw r1, 0(r1) |  |  |  | F | D | E | M | W |  |  |  |  |  |  |  |
| beq r1, r0, loop |  |  |  |  | F | D | E | M | W |  |  |  |  |  |  |
| (4th) |  |  |  |  |  | F | D | E | M | W |  |  |  |  |  |
| (4th) |  |  |  |  |  |  | F | D | E | M | W |  |  |  |  |
| (4th) |  |  |  |  |  |  |  | F | D | E | M | W |  |  |  |
| (4th) |  |  |  |  |  |  |  |  | F | D | E | M | W |  |  |
| (4th) |  |  |  |  |  |  |  |  |  | F | D | E | M | W |  |

1. [5pts]How often (as a percentage of all cycles) do we have a cycle in which all five pipeline stages are doing useful work?

It takes 9 clock cycles for one loop of the program to fully execute (from the first instructions first active clock cycle to the 5th instruction’s final active clock cycle, highlighted above). One of these has all 5 pipeline stages doing useful work. Therefore, the percentage for this is 1/9 = **11.11%**

1. Branch prediction, accuracy and impact.

The CPI for an ideal 5-stage pipeline that is always full is 1. Assume a code with no data hazards, and no delay slots are used, but with 25% of branch instruction. Assume that branch outcomes are determined in the ID stage and a misprediction causes a cycle delay. Also assume the following branch predictor accuracies.

|  |  |  |
| --- | --- | --- |
| Always-Taken | Always-Not-Taken | 2-Bit |
| 45% | 55% | 85% |

1. [5pts]Stall cycles due to mispredicted branches increase the CPI. What is the extra CPI due to mispredicted branches with the always-taken predictor?

**1.275**

1. [5pts]What is the extra CPI due to mispredicted branches with the always-not-taken predictor?

**1.225**

1. [5pts]What is the extra CPI due to mispredicted branches with the 2-bit predictor?

**1.075**

1. [20pts]Based on the lecture notes, you are given a standard single issue 5-stage pipeline with forwarding, extended with an integer ALU and a floating-point ALU (integer instructions executing as 'E' and FP instructions executing as 'X' respectively). An independent instruction can start into the execute stage on each cycle. All instructions must complete in program order, so single-cycle instructions cannot enter the memory stage until all previous instruction have passed through the memory stage.

E.g.,

and

addf F4,F2,F0 //4-cycle fp exec, F4 <- F2 + F0 F D X X X X M W

addf F8,F6,F0 //4-cycle fp exec, F8 <- F6 + F0 F D X X X X M W

addf F4,F2,F0 //4-cycle fp exec, F4 <- F2 + F0 F D X X X X M W

sub R1,R1,16 //1-cycle int exec, R1 <- R1 - 16 F D E - - - M W

1. [15pts]Given the following loop code segment, draw the pipeline diagram in the table by filling the stages and stalls, and mark the data forwarding.

Loop: ld F0, 0(R1) // 1-cycle latency, F0 <- memory[ R1 + 0 ]

addf F4, F2,F0 // 3-cycle latency, F4 <- F2 + F0

st F4, 0(R1) // 1-cycle latency, memory[ R1 + 0 ] <- F4

ld F6, 8(R1) // 1-cycle latency, F6 <- memory[ R1 + 8 ]

addf F8, F6,F0 // 3-cycle latency, F8 <- F6 + F0

st F8, 8(R1) // 1-cycle latency, memory[ R1 + 8 ] <- F8

sub R1, R1, 16 // 0-cycle latency, R1 <- R1 - 16

bne R1, R2, loop // 0-cycle latency, branch to loop if R1 != R2

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |
| Loop: ld F0, 0(R1) | F | D | E | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| addf F4, F2, F0 |  | F | D | X | X | X | X | M | W |  |  |  |  |  |  |  |  |  |  |  |  |
| st F4, 0(R1) |  |  | F | D | E | - | - | - | M | W |  |  |  |  |  |  |  |  |  |  |  |
| ld F6, 8(R1) |  |  |  | F | D | E | - | - | - | M | W |  |  |  |  |  |  |  |  |  |  |
| addf F8, F6, F0 |  |  |  |  | F | D | X | X | X | X | M | W |  |  |  |  |  |  |  |  |  |
| st F8, 8(R1) |  |  |  |  |  | F | D | E | - | - | - | M | W |  |  |  |  |  |  |  |  |
| sub R1, R1, 16 |  |  |  |  |  |  | F | D | E | - | - | - | M | W |  |  |  |  |  |  |  |
| bne R1, R2, loop |  |  |  |  |  |  |  | F | D | E | - | - | - | M | W |  |  |  |  |  |  |

1. [5pts]How many cycles are there between two successive stores of F4 in the loop? Consider there is no branch prediction.

**F4 is only used in instructions 2 and 3. Between the storing stages of each of those instructions, there is only 1 cycle difference. So there is 1 cycle between successive stores of F4.**

1. 2-issue processors. You are given the following code for a loop:

Loop: lw r1, 0(r6)

lw r2, 4(r6)

sub r3, r1, r2

sw r3, 0(r7)

addi r6, r6, 8

addi r7, r7, 8

addi r4, r4, 2

bne r4, r0, loop

1. [15pt]If the loop exits after executing only two iterations. Show the scheduled instructions for the given MIPS code on a 2-issue processor shown in Figure 4.69. Assume the processor has perfect branch prediction.

|  |  |  |  |
| --- | --- | --- | --- |
| loop | ALU/branch | Load/store | cycle |
| 1st iteration |  | lw r1, 0(r6) | 1 |
|  |  | lw r2, 4(r6) | 2 |
|  | sub r3, r1, r2 | sw r3, 0(r7) | 3 |
|  | addi r6, r6, 8 |  | 4 |
|  | addi r7, r7, 8 |  | 5 |
|  | addi r4, r4, 2 |  | 6 |
|  | bne r4, r0, loop |  | 7 |
| 2nd iteration is the same |  |  |  |

1. [15pts]Rearrange the code to achieve better performance on a 2-issue statically scheduled processor from Figure 4.69. Write the sequence below.

**Loop: lw r1, 0(r6)**

**addi r4, r4, 2**

**lw r2, 4(r6)**

**sub r3, r1, r2**

**sw r3, 0(r7)**

**addi r6, r6, 8**

**addi r7, r7, 8**

**bne r4, r0, loop**

1. [15pts]Repeat step a for the code from b.

|  |  |  |  |
| --- | --- | --- | --- |
| loop | ALU/branch | Load/store | cycle |
| 1st iteration | addi r4, r4, 2 | lw r1, 0(r6) | 1 |
|  | sub r3, r1, r2 | lw r2, 4(r6) | 2 |
|  | addi r6, r6, 8 | sw r3, 0(r7) | 3 |
|  | addi r7, r7, 8 |  | 4 |
|  | bne r4, r0, loop |  | 5 |